

Customer No.: 31561
Docket No.: 10465-US-PA
Application No.: 10/707,354

REMARKS

Claims 1-18 are pending of which the claims 1, 2 and 5 have been amended, the claim 6 has been cancelled and the claims 9-18 have been added without prejudice or disclaimer in order to more explicitly describe the claimed invention. It is believed that no new matter is added by way of amendments made to claims or otherwise to the application. For at least the foregoing reason, Applicants respectfully submit that claims 1-18 patently define over prior art of record and reconsideration of this application is respectfully requested.

In The Specification

Applicants appreciate that the examiner pointed out all grammar errors occurred in the specification, as well as in the "ABSTRACT." Therefore, applicants amended all the grammar errors. Besides, the inconsistencies between the amended claims and the specification were amended as well. Enclosed please a copy of the marked up the specification, in which the added portion were underlined and the deleted portion were crossed out through a line. A clean copy of the specification is also enclosed.

Discussion of the added claims 9-18

The added claims 9-18 were added without introducing any new matter. Further, the added claim 9 is supported in Fig.2 and the paragraph [0013] in the amended specification, so does the added claim 10. Moreover, the added claim 11 is supported in

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the second sentence in the paragraph [0018] in the amended specification, and the added claims 12-16 are supported in the amended specification.

Discussion of objection to Specification

3. The disclosure is objected because of the following informalities: the specification is replete with grammatical errors to mention specifically.

In response thereto, enclosed please find one marked version and clean version of the specification, respectively. In the marked version of the specification, the amended portion in the amended specification, the amended claims and the amended abstract are underlined while the clean version of the specification is a most updated version

Discussion for objection to claims under 35U.S.C. 102(e)

4. Claims 1-6 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. 6,777,986 (Hidaka, hereinafter referred to Hidaka)

As to claims 1,2 , note Fig.3, where the recited "main output stage" reads on the push-pull of FETs 1a and 2a; the recited "monitoring stage" reads on the combination of delay 12b and gates 13b,14b; and the recited "assistant output stage" reads on the push-pull of FETs 1b,2b.

As to claims 5,6, note Fig.80A, where the detecting of the first and second inputs occurs due to the action of differential amplifier 490; the push/pull currents are

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through the FETs 492 and 494, respectively; the feedback of the push/pull currents (claim 6) is from the common drain of the FETs 492 and 494 to the non-inverting input of amplifier 490.

In response thereto, applicants respectfully traverse the preceding examiner's objections to the claims based on the following arguments, and reconsideration of the amended claims 1-15 is respectfully requested.

To establish a prima facie case of anticipation, the cited reference (i.e. Hidaka) should teach, suggest or disclose all limitations of the independent claims 1, 5 and 9. From lines 4-5, in paragraph [0018], in the amended specification, there discloses "even a voltage at the inverting input is equal to that at the non-inverting input, there exists a quiescent DC biased current at the node N₂₂." The independent claims 1, 5 and 9 are accordingly amended. Hence, first of all, Hidaka fails to teach, suggest or disclose "the main current further comprises a quiescent DC biased current" as claimed in the amended independent claims 1, 5 and 9. This is because Hidaka operates as a logic circuit, as verified from the claims 1 and 2, so that the main current as alleged by the examiner must be either the zero current with the "0" logic level or a current with the "1" logic level.

Secondly, in Fig.3, the monitoring stage as alleged by the examiner has only one output connected to the assistant stage as alleged by the examiner. As a result, Hidaka fails to teach, suggest or disclose "a first output and a second output of the monitoring stage are connected to the gate of the third field effect transistor with the first type and the gate of the fourth field effect transistor with the second type, respectively, so as to output

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stage are connected to the gate of the third field effect transistor with the first type and the gate of the fourth field effect transistor with the second type, respectively, so as to output the decayed push signal and the decayed pull signal to the assistant output stage.” as claimed in the amended independent claims 1, 5 and 9.

Thirdly, in Figs 1 and 3, as well as in col. 10, line 35 and col. 6, line 53, there disclose the FETs 1a, 1b, 2a and 2b are all n channel MOS transistors. As a result, Hidaka fails to teach, suggest or disclose” either of the main output stage and the assistant output stage comprises one field effect transistor with the first type and another field effect transistor with the second type” as claimed in the amended independent claims 1, 5 and 9.

Accordingly, Hidaka fails to teach, suggest or disclose all limitations of the amended independent claims 1, 5 and 9. In other words, the amended independent claims 1, 5 and 9 are not anticipated by Hidaka and thus patentable over Hidaka under 35 U.S.C. 102 (e).

Regarding dependent claims 2-4, 6-8, 10-15, no matter whether they are conventional, they should be patentable as a matter of law for the reason they must contain all limitations of their corresponding allowable independent claims 1, 5 and 9.

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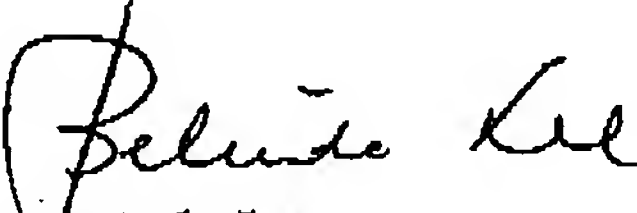
CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-18 of the invention patently define over the prior art and are in proper condition for allowance. Reconsideration of claims 1-18 and the present application is respectfully requested. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,

Date :

August 16, 2005


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